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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/413,177	10/07/1999	LAP CHAN	CS99-107	1672

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/413,177	CHAN ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,5,6,8-18 and 22* is/are rejected.

7)☒ Claim(s) *3,4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 15 – 17, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (USPAT 5413962, Lur) in view of Staudinger et al. (USPAT 5481131, Staudinger).

Lur discloses a method of forming air gaps within an integrated circuit structure in figures 1 – 11.

With regard to claim 1, Lur discloses in figure 1 providing a partially fabricated integrated circuit structure (20, 22 – 24, and 28) and depositing a layer of dielectric (30) thereon. Lur discloses in figure 1 forming a metal layer (40) on the dielectric layer. Lur discloses in figure 1 depositing a first thin layer of oxide (bottom most, 42) over the dielectric layer, thereby including the metal layer. Lur discloses in figures 2 – 7 forming a structure for first cavities over the first thin layer of oxide and aligned with the metal layer, the forming a structure for first cavities comprising applying (bottom most, 34) and patterning (27) a first layer of disposable solid followed by applying (third from bottom, 42) and patterning (processing between figures 6 and 7) a first layer of oxide, the patterning a first layer of oxide further comprising forming a

first (between the second and third from left, "51's") and a second (between the fourth and fifth from left, "51's") opening through said first layer of oxide. Lur discloses in figures 9 and 10 forming a structure for second cavities above and aligned with the structure for the first cavities the forming a structure for second cavities comprising applying (top most, 34) and patterning (top via defining topmost contact 29) a second layer of disposable solid followed by applying (topmost 42) and patterning (figure 10) a second layer of oxide, the patterning a second layer of oxide further comprising forming a first (space between left most 70's) and a second (space between right most 70's) opening through said second layer of oxide. Lur discloses in figure 11 creating the first (bottom most section of 85) and the second (top most section of 85) cavities. Lur discloses in figure 11 performing an oxide (80) deposition over the surface of the second cavities creating a second thin layer of oxide. Lur does not disclose forming a metal inductor on the surface of the second thin layer of oxide. Staudinger teaches in figure 2 forming a metal inductor (21) on a surface of a thin second layer of oxide (36). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the metal inductor of Staudinger on the second thin oxide of Lur in order to optimize the size and weight of the semiconductor device by integrating both active and passive components onto the same chip as stated by Staudinger in column 1, lines 12 – 26.

With regard to claim 2, Lur discloses in figure 1 the forming a metal layer on the surface of the dielectric layer is forming the metal layer having the cross section of a square or a rectangle having vertical sides.

With regard to claim 5, Lur discloses in figures 10 and 11 that the creating a first and a second layer of cavities is removing the first and second layer of disposable solid, the removal to

take place by accessing the first and second layer of disposable solid by means of the first and second openings created in the second layer of oxide furthermore by accessing the first layer of disposable solid by means of the first and second openings in the first layer of oxide, creating a first layer and a second layer of dielectric comprising horizontal oxide fins (layers of oxide 42 after removal of disposable solid), further creating a first layer and a second layer of horizontal air gaps being interspersed with the first layer and a second layer of dielectric.

With regard to claim 6, Lur discloses in figures 10 and 11 that the performing an oxide deposition over the second layer of cavities is creating a thin layer of oxide over the second layer of oxide thereby furthermore closing the first and the second openings created in the second layer of oxide.

With regard to claims 15, Staudinger teaches in figures 13 – 15 that the inductor is spiral shaped.

With regard to claims 16, Staudinger teaches in figures 13 – 15 that the inductor is circular shaped.

With regard to claim 17, Staudinger teaches in figures 13 – 15 the polygonal inductor is an octagon.

With regard to claim 22, Lur discloses in figures 10 and 11 the layers of disposable solid being layers of nitride.

3. Claims 8 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of Havemann et al. (USPAT 5668398, Havemann).

Lur and Staudinger do not teach that the disposable solid comprises a polymer.

With regard to claim 8, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 a disposable solid that comprises a polymer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the polymer of Havemann as the first and second disposable solids of Lur and Staudinger in order to form air gaps between metal leads of a semiconductor device using a class of materials that has a wide range of process flexibility based on material selection and process parameters.

With regard to claim 9, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 the creating cavities is heating the substrate in oxygen, evaporating the disposable solid layer using O_2 plasma.

With regard to claim 10, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 the creating a layer of cavities is introducing a solvent to the substrate dissolving the polymer.

With regard to claim 11, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 wherein creating a first and a second layer of cavities is heating the substrate, evaporating the polymer.

With regard to claim 12, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 wherein creating cavities is applying a vacuum to the substrate, dissolving the polymer.

It would further be obvious that Havemann applies to both the first and second disposable solids of Lur and Staudinger.

4. Claims 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of Abidi et al.

With regard to claim 13, Lur and Staudinger do not disclose an insulating layer deposited over the surface of the inductor. Abidi et al. teaches in figures 6a – 6c depositing an insulating layer (20) over the surface of an inductor (76) thereby encapsulating the inductor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the insulating layer of Abidi et al. to encapsulated the inductor of Lur and Staudinger in order to insulated the inductor from surroundings outside of the chip as is well known in the art.

With regard to claim 18, Lur and Staudinger do not specify properties of the inductor. Abidi et al. discloses in column 7, lines 34 – 37 an inductor having an inductance in excess of 1 nh and a self-resonance in excess of 10 MHz. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use an inductor with the disclosed properties of Abidi et al. in the method of Lur and Staudinger in order to have an RF tuned amplifier that can be fabricate having a large value monolithic inductor thereby substantially increasing as stated by Abidi et al in column 7, lines 35 – 42.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of one of ordinary skill in the art.

It is not clear if the partially fabricated integrated circuit structure of Lur and Staudinger comprising transistors being CMOS and are interconnected to form an RF amplifier. It is well known in the art to form partially fabricated integrated circuit structures that are transistors being CMOS interconnected to form an RF amplifier. It would have been obvious to one of ordinary

skill in the art at the time of the present invention to use have the devices of Lur and Staudinger bet CMOS transistors in RF amplifier circuits in order to create a circuit that has exceptionally high input impedance (e.g. megohms), square law transfer characteristics which result in low cross modulation products, and wide dynamic operating range.

Allowable Subject Matter

6. Claims 3, 4, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed December 8, 2003 have been fully considered but they are not persuasive.

8. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore the applicant's arguments are not persuasive and the rejection is proper.

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., dielectric of air surrounding interconnect metal...) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore the applicant's arguments are not persuasive and the rejection is proper.

10. With regard to the applicant's argument that the "processes of Figs. 1 – 11 are believed to be both novel and patentable over these various references," it should be noted that the claims, not the figures, need to be both novel and patentable over the references. Therefore the applicant's arguments are not persuasive and the rejection is proper.

11. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, all of the combinations of references have appropriate motivations to combine. In all such above combinations the motivation may be found after the phrase "...in order to...". Applicant has not pointed out specifically why any of these motivations fail. Therefore, applicant's arguments are not persuasive, and the rejections are proper.

12. With regard to applicant's argument that none of the references "provide for the creation of horizontal air gaps that are interspersed with layers of dielectric while further none of the inventions provide for a method of removal of a disposable solid, such as nitride, for the creation of the air gaps as claimed in the claims of the instant invention," it should be noted that these features are not claimed in independent claim 1. Further, these features are disclosed by primary reference Lur. Therefore, applicant's arguments are not persuasive, and the rejections are proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II